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February 3, 2004

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Applicant(s): Satwant Singh; Cyrus Tsui
Assignee: Lattice Semiconductor Corporation
Title: Delay-Matched ASIC Conversion Of A Programmable Logic Devices
Serial No.: 10/660,814 Filed: 09/12/2003
Examiner: Unknown Group Art Unit: 2819
Docket No.: M-15198 US

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- (1) Return Receipt Postcard;
- (2) This Transmittal Letter (in duplicate);
- (3) Submission of formal drawings with five (5) sheets of formal drawings including Figures 1, 2, 3, 4a, 4b, 5, 6, and 7;
- (4) Information Disclosure Statement; and
- (5) PTO-1449 with copies of three (3) cited references.



No additional fee is required.



The fee has been calculated as shown below:

CLAIMS AS AMENDED

	Claims Remaining <u>After</u> <u>Amendment</u>		Highest No. Previously <u>Paid</u> <u>For</u>		Present <u>Extra</u>		<u>Rate</u>		<u>Additional Fee</u>
Total Claims	37	Minus	37	=	0	x	\$18.00	\$	0
Independent Claims	5	Minus	5	=	0	x	\$86.00	\$	0
<input type="checkbox"/>	Fee of _____ for the first filing of one or more multiple dependent claims per application								\$
<input type="checkbox"/>	Fee for Request for Extension of Time								\$

Total additional fee for this Amendment:

\$



Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.



Please charge our Deposit Account No. 50-2257 in the amount of \$



Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 50-2257

Total: \$

0

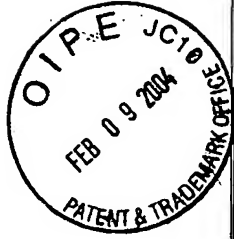
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 3, 2004.

Eric Hoover

February 3, 2004
Date of Signature

Respectfully submitted,

Jon W. Hallman
Attorney for Applicants
Reg. No. 42,622



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Satwant Singh; Cyrus Tsui
Assignee: Lattice Semiconductor Corporation
Title: Delay-Matches ASIC Conversion Of A Programmable Logic Devices
Serial No.: 10/660,814 Filing Date: 09/12/2003
Examiner: Unassigned Group Art Unit: 2819
Docket No.: M-15198 US

Irvine, California
February 3, 2004

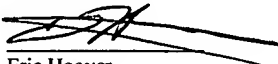
Attn: Official Draftsperson
COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit five (5) sheets of formal drawings, consisting of Figures 1, 2, 3, 4a, 4b, 5, 6, and 7, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (949) 752-7040.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on February 3, 2004.


Eric Hoover

February 3, 2004

Respectfully submitted,



Jon W. Hallman
Attorney for Applicants
Reg. No. 42,622

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Satwant Singh; Cyrus Tsui
Assignee: Lattice Semiconductor Corporation
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February 3, 2004

COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

UNDER 37 C.F.R. §1.97 AND § 1.98

Dear Sir:

Pursuant to 37 C.F.R. §1.97 and §1.98, Applicant calls the following documents (copies enclosed) to the attention of the Examiner. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

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2. a representation that a search has been made, or
3. an admission that the information cited herein is, or is considered to be material to patentability as defined in §1.56(b).

Applicant(s) believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 50-2257. Please deduct any additional fees from, or credit any overpayment to the above-noted Deposit Account.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on February 3, 2004.



Eric Hoover

February 3, 2004

Respectfully submitted,



Jon W. Hallman
Attorney for Applicant(s)
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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15198 US	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant(s)	
	Satwant Singh; Cyrus Tsui	
	Filing Date	Group
	09/12/2003	2819

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AL						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AQ	Altera Hard Copy, Devices for APEX 20K Conversion, Data Sheet, September 2001, ver. 1.0, pages 1-36
AR	XPressArray 0.18 μ Hybrid Gate Array, AMI Semiconductor, pages 1-8
AS	PGA Data Book, October 1996, Masked Array Conversion For ORCA ("MACO"), Lucent Technologies Inc.

Examiner	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.